DOI: 10.15415/jtmge.2016.72007

Green Computing

Jagwinder Singh
Chitkara University, Punjab, India.

Abstract

Green Computing is the concept to improve environmental conditions. Green Computing has begun to spread in the past few years, gaining increasingly popularity. It includes manufacturing, designing and efficiently using computers and associated subsystems- such as LED,RAM, Processor, Mouse and Keyboard with minimum impact on the environment. We are doing the study and practice of developing Information Technology resources in an environment friendly manner such that our environment get protected. As we all know usage of electronic devices is very popular these days, of which Laptops and Tabs are the most common. Surveys were conducted to analyze power consumption, pattern of devices, components like RAM, Rom processors and LED displays. Furthermore recommendations were made to make them more energy efficient. To promote the idea of green computing, energy star rating were introduced for electronic devices. The more is the star rating, the less is the power consumption. This type of computing can facilitate us to safe and make healthy environment all over the world. Present study will help us to take some initiatives to save vast amount of power which is wasted on very large scale currently under the field of computers/ electronics industry.

Keywords: *Green Computing, energy efficient, Power consumption*

INTRODUCTION

Green Computing refers to the method of using environmentally sustainable computers accessories and our aim is to design, manufacture, and disposal of computers with minimum or no impact on the environment. Green IT is used to explain the use of eco-friendly devices in Information Technology. Green computing will promote the recycling of electronic components and parts.

Energy efficiency is increasingly important for future ICT (Information and Communication Technologies) related to the cost, and availability of energy is rising day by day. The main emphasis is to reduce greenhouse gas emissions demand for energy-efficient technologies that decrease the overall energy consumption of computation, storage and communications.

As the time passes focus of enterprises and technology firms has been shifted towards Green Computing rapidly. It discusses the options to support critical computing needs in sustainable manner by reducing strains on resources and environment.

Many efforts have been done in this area to improve the power efficiency of the PC components and making the IT sector energy savior so that green computing can be accomplished. One of the main and the

Journal of Technology Management for Growing Economies
Vol. 7, No. 2
October 2016
pp. 127-142

primary objective of Green Computing is about improving computing performance and reducing the energy consumption. This was the real motivation behind proposing optimized power guzzling IT devices. An example of green computing practice can be, witness as sleep mode in modern computers.

LITERATURE REVIEW

The literature review was undertaken the foundations of this research. Literature review includes journals, publications, magazines, books and technical reports from renowned organizations leading the green computing industry.

Telikepalli Anil and I. Xilinx[30] , 2003 spotlight on security in our planet, it is quite obvious for us to stress over the security of our designs. Xilinx proves to be a secured software. Here at Xilinx, we need to sit back and relax. All Xilinx gadgets (FPGA's and CPLD's) have strong security systems that make it almost difficult to steal our designs. Specifically, Virtex-II Pro Platform FPGAs have propelled Triple DES (Data Encryption Standard) Security. Triple DES calculations give the same security that the world's monetary organizations depend on consistently for exchanges including trillions of dollars. With security instruments you "bank" on, how about we dive into the subtle elements of design security and how Xilinx ensures your significant exclusive plans.

Aqeel Mahesri, Vibhore Vardhan [31], 2005 calculated the component wise power consumption of the individual components of IBM R40 Thinkpad laptop using an Agilent Oscilloscope. Power consumed by the optical drive, CPU, Display, hard drive, memory, wireless and graphic card subsystem was calculated. Power was measured after making variations in the workload. It was observed that the power fluctuated between 8-30W depending on the workload. Different power saving techniques was used to minimize the power consumption. In case of display, power can be reduced by dimming the backlight of the system. For CPU power saving technique named DVS was used. Finally it was observed that major power consumption depends on Operating System that we are using.

For measuring power consumption, the author used five steps:

1. The system was broken down into various components and sub components so that it could work with minimum configurations.
2. Measuring the power consumption of each component directly.
3. Several benchmarks were run and components wise power consumption was determined.
4. Power consumption of whole of the system was determined.

5. Power consumption under workloads was determined

D. Wang [16], 2008 suggested that green maintainability is just not the utilization of operational energy of processing hardware. Green computing also takes the item's life cycle into thought, from its generation to operation till its reusage. The study concentrated on the creation and the operation periods of the item life cycle and exhibited what activities will bring about lessened carbon footprint for individual and business computations under different operational conditions and situations. Energy utilization with end of life item reusage is not talked about in this study and is not accepted to significantly affect the operational energy and carbon impression.

S. Murugesan[27] ,2008 says that moving towards a greener course and utilization of other ecology activities, IT is making everything greener. Overall population is being helped in one way or the other- building groups, drawing artists and supporting training groups. Green IT is a financial, and in additional natural, basic. Greening IT is and will keep on being a need, impossible. Green IT speaks to a sensational change in need in the IT business. In this way ,the industry has been worried with different prerequisites, For example, Force, cooling and server farm space. Be that as it may, going ahead, the IT business should manage the majority of the base prerequisites and the ecological effect of IT and its utilization.

Andreas Berl and Erol Gelenbe[32], 2009 presented that energy efficiency is progressively essential for future information and communication innovations under (ICT), on the grounds that the expanded use of ICT, together with expanding energy costs and the need to diminish green house gas emanations call for energy efficient advancements that lessening the general power utilization of calculations, stockpiling and interchanges.

Binder Walter and Niranjan Sure[33]. 2009 concentrated on green computing in making designs, building and working PC frameworks energy proficient. The worry with respect to worldwide environmental change and energy emergency led to the research in the field of green computing. For this purpose, energy star rating came in around early 1990's. Data centers came to be known as major energy consumers both to provide power to centers as well as computers. The paper proposed wonderful techniques to minimize the energy utilization of the servers and data centers.

OBJECTIVES AND METHODOLOGY

The other emissions and CO2 are causing environmental damage globally. Reduction in the power consumption can indirectly reduce the carbon emissions

in the environment. Hence it is intended to design an environment friendly electronic gadget which should be more power efficient than present devices.

To overcome the challenges emerged by the use if devices that are power guzzlers, it is intended to reduce the carbon traces in the environment by uplifting/ remodeling the system software for electronic devices. The carbon traces based on the power consumption can be formulated as:

If x Kg coal produces y W power. If a design uses y W power then its impact on the environment is consumption of x kg non-renewable resource like coal. Using energy efficient technique, if we are able to save 50% power then it mean we are saving x/2 kg coal.

Objectives

1. To identify major power consuming components within electronic devices like computers and smart phones.
2. To simulate hardware performance of identified components on XILINX, so as to lessen their power consumption.
3. To analyze the anticipated green impact of redesigned hardware components on natural resources i.e. carbon footprints.

METHODOLOGY

Phase-1

Need to find out major power consuming components within electronics devices like computers and smart phones. The embedded software for major power guzzling electronic components would be coded using XILINX.

Phase-2

To simulate hardware performance of identified components on XILINX. The embedded software code for identified electronic components would be redesigned with an intension to reduce their power consumption. The cumulative effect of redesigned embedded software on the power consumption of the entire system would be calculated.

Phase-3

To analyze the anticipated green impact of redesigned hardware components on natural resources i.e. carbon footprints: Effect of redesigned power efficient electronic components on carbon footprints would be calculated using online carbon footprint calculators.

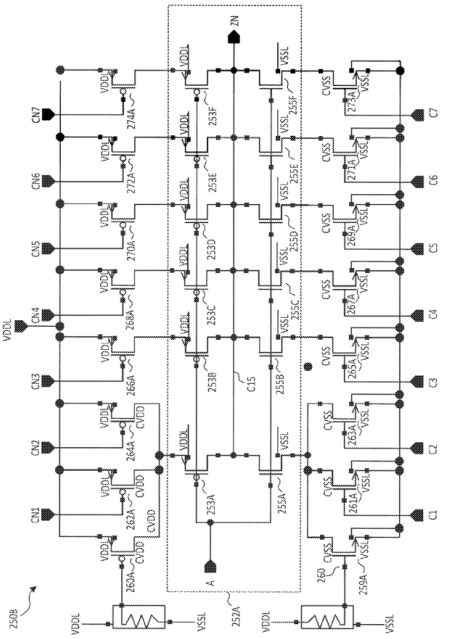

Figure 1. RTL Schematic Processor

RTL Schematic of LED Display

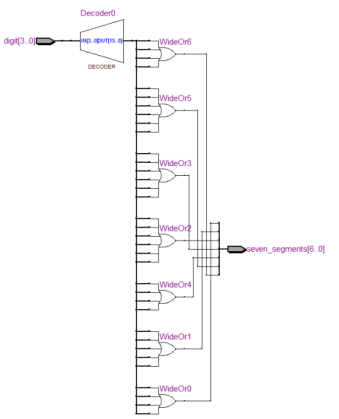

Figure 2. RTL Schematic LED Display

INPUT OUTPUT STANDARD

The Input Output Standard limitation is an essential mapping and union requirement. Field Programmable Gate Arrays (FPGA's) are equipped for supporting an assortment of various Input/ Output (IO) standards.
Choice of IO standard proves to be an essential part in improving the power efficiency of general configuration.

The 8 bit processor in figure input 8 bit signal and output an 8-bit data signal. According to the clock signals provided it outputs the appropriate data. IRQ is the interrupt request. If some request has the higher priority it is send using IRQ and is processed first.

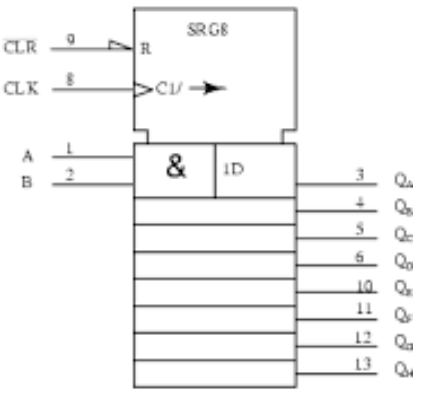

Figure 3: RTL Design of Processor

Below Figure 4 accepts the 4 bit input through 4 different input ports and outputs a 4 bit data output. The output is recorded as 7 bits.

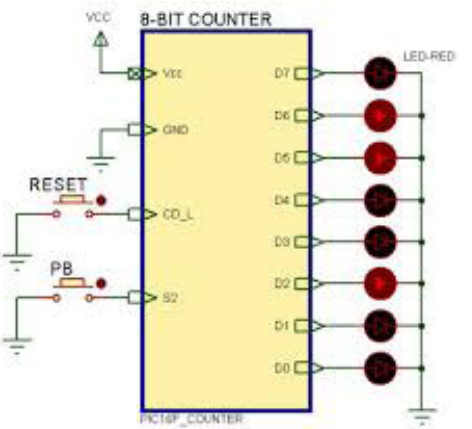

Figure 4: RTL Design of LED Display

LVCMOS

Low Voltage Complementary Metal Oxide Semiconductor operates on the lowest voltage and it is most productive and is known for lowest power dissipation. LVCMOS is used to implement the CMOS logic.

HSTL(High Speed Transceiver Logic)

The HSTL standard is also defined by JEDEC. The HSTL standard have four variations (classes) [11]. This is used to link general purpose high speed buses. Differential versions of HSTL IO standards are also available interface the high speed memory links. FPGA I/O provides 1.2 V version of HSTL in class-I, and 1.5 V and 1.8 V versions for both classes of HSTL IO standard. A Differential amplifier and a push pull buffer are also used as input buffer and output buffer respectively in differential versions of HSTL IO standard. These are two power banks in FPGA one is (High Performance) and other is HR (High Range). The application of HSTL class I IO standard are unidirectional connections.

HSTL II IO standard uses $V_{cco}/2$ as a parallel termination voltage (VTT). It can be using the bidirectional links.

RESULTS AND DISCUSSIONS

Process Scaling

Process variation is related to fabrication of Integrated Circuit (IC). To calculate effect of total power on considered design, the design is implemented on 40 nm and o fulfil our purpose we are using Viretex-6

Total power analysis of different PC components using LVCMOSIO Standard. The standard is stated in JEDEC (JESD 8C.01). LVCMOS is available in following types in 7 series FPGAL LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15 and LVCMOS12. Emphasis in this work, is on LVCMOS12 and LVCMOS15. Power analysis of PC components using different IO standards on 40nm FPGA is done. These tables show the effect of voltage scaling on multiple IO standards. In this work, total power dissipation is measured on different processor frequencies (I3,I5,I7) as shown in table 1 below.

Table 1: Processor's operating Frequencies

Processor	Frequency (GHz)
I3	2.5
I5	3.6
I7	3.0

Total power analysis of processor at different Frequencies using different I/O standards

Power dissipated by processor at 1.2 GHz operating frequency:

A processor is a device that reacts to and from the fundamental directions that drive a PC.

Table 2: Power Dissipated by a Processor at 1.2 GHZ operating Frequency

IO Standards	Clock	Logic	Signal	Ios	Leekage	Total
LVCMOS12	0.02	0.006	0.016	0.15	0.34	0.532
LVCMOS15	0.028	0.009	0.021	0.282	0.323	0.663
HSTL_I	0.027	0.006	0.018	0.27	0.325	0.646
HSTL_II	0.027	0.006	0.018	0.29	0.326	0.667

On 1.2 GHz a reduction of 2.22% in the clock power, 20% reduction in the logic, 28% reduction in the signal power, 46.68% reduction in the Ios power is observed.

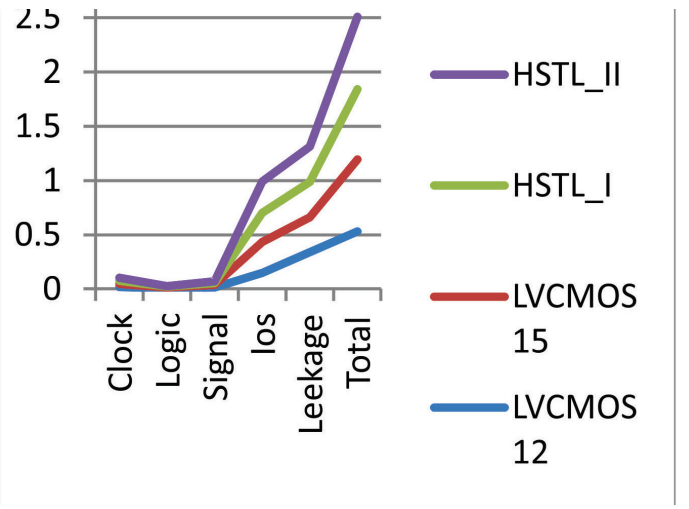

Figure 5: Power Dissipation on 1.2 GHz

Also 0.90% decline in the leakage power is observed when we are using LVCMOS12 instead of HSTL_I as shown in figures. Finally, we get 21.70% reduction in the total power when LVCMOS12 is used.

POWER DISSIPATED BY PROCESSOR AT 1.7 GHZ OPERATING FREQUENCY

Total power dissipation on 8 bit processor is calculated using different IO standard is found. As LVCMOS[6] operates on the lowest voltage and it is most productive and is known for the lowest power dissipation so it is found that LVCMOS is the best standard.

Table 3: Power Dispersion by a processor at 1.7 GHz

IO Standard	Clock	Logic	Signal	Ios	Leekage	Total
LVCMOS12	0.04	0.03	0.02	0.218	0.319	0.627
LVCMOS15	0.04	0.01	0.03	0.387	0.319	0.786
HSTL_I	0.049	0.03	0.024	0.309	0.32	0.732
HSTL_II	0.049	0.02	0.024	0.324	0.32	0.737

After applying an I/o standard LVCMOS12 on 1.7 GHz processor, decline of 15.65% is observed in clock power and decline of 21.07% is observed in logic power and 28.80% in signal power as shown in the figure 6 and table 3. Also IO power is depreciated by 42.44%,leakage power by 0.90%

Thus total power Is depreciated by 21.79% when LVCMOS12 is used instead of HSTL_II as shown above.

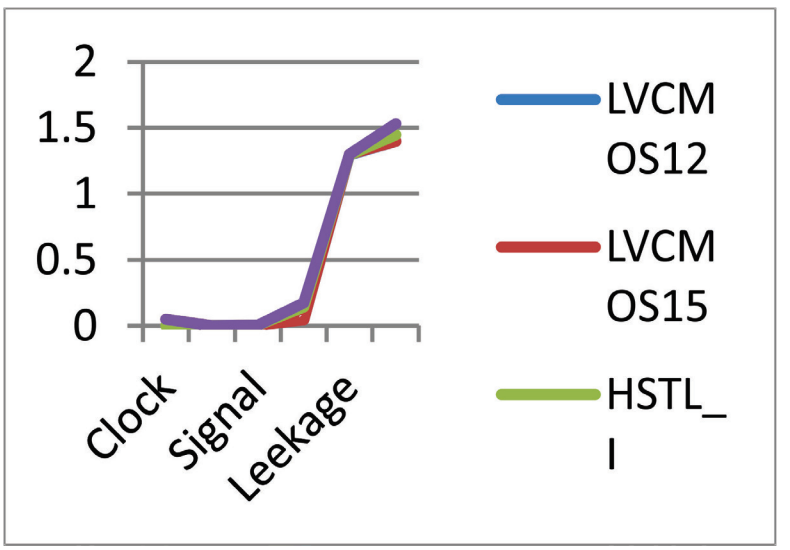

Figure 6: Power Dissipated by a processor at 1.7 GHz

POWER DISSIPATED BY A PROCESSOR AT 2.5 GHZ OPERATING FREQUENCY

On Frequency reduction of 2.5 GHz Frequency, signal power by applying I/O standard LVCMOS12 is observed as 22.12% , 25%, 27.45%. Minimization in leakage power and IO's power is 1.20% and 42.30%. As a result reduction of 26.97% in the total power is observed when LVCMOS12 is used instead of different HSTL IO standards as shown in figures and tables.

Power Dispersion by a processor at 2.5 GHz Figure 7 **Power Dissipated by a processor at 2.5 GHz**

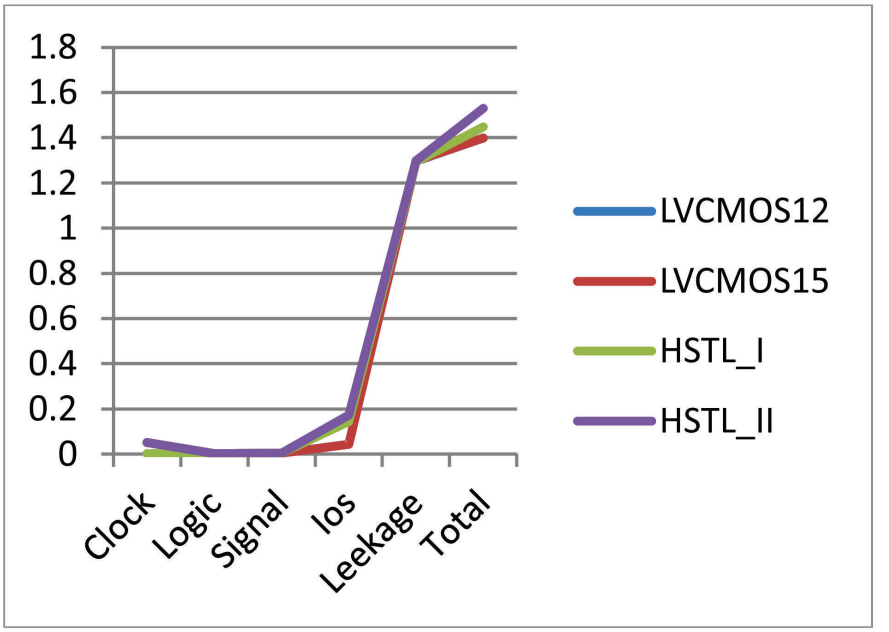

Figure7: Power dissipation by a processor on 2.5 GHz

In figure 7 X axis depict the values of power and Y axis represents the values for different IO standards and by using LVCMOS12 we save 25.67% total power. We conclude that LVCMOS is the best IO standard as compared to LVCMOS15, HSTL_I and HSTL_II.

POWER DISSIPATED BY PROCESSOR AT 3.0 GHZ OPERATING FREQUENCY

This table shows power analysis of processor using LVCMOS and HSTL IO standards on Virtx-6 using process scaling technique

Table 4: Power Dissipation by a processor at 3.0 GHz

IO Standard	Clock	Logic	Signal	Ios	Leekage	Total
LVCMOS12	0.082	0.011	0.034	0.321	0.32	0.768
LVCMOS15	0.11	0.021	0.049	0.58	0.324	1.084
HSTL_I	0.09	0.011	0.039	0.37	0.321	0.831
HSTL_II	0.095	0.011	0.042	0.358	0.321	0.827

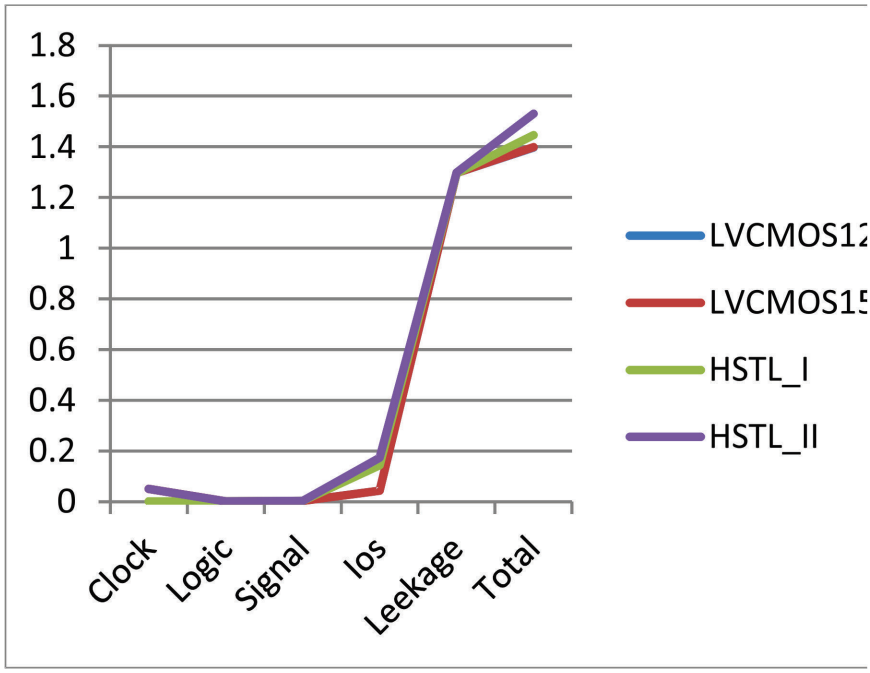

Figure 8: Power Dissipation by a processor at 3.0GHz

On 3.0 GHz Frequency decrement in clock power (17.03%), logic power (20.70%), signal power (26.33%) is analyzed as shown in figure 8 and table 4

TOTAL POWER ANALYSIS OF DISPLAY AT DIFFERENT FREQUENCIES USING DIFFERENT IO STANDARDS

Power Dissipated by display at 1.2 GHz operating Frequency

The RTL of the display design accepts 4 bit input and converts it into 7 segments pixels. The table shown depicts the total power using different input output standards.

Table 5: Power Dispersion by LED Display at 1.2 GHz

IO Standard	Clock	Logic	Signal	Ios	Leekage	Total
LVCMOS12	0.036	0	0.003	0.026	1.286	1.351
LVCMOS15	0.036	0	0.003	0.024	1.286	1.349
HSTL_I	0.036	0	0.003	0.147	1.291	1.477
HSTL_II	0.036	0	0.003	0.175	1.291	1.505

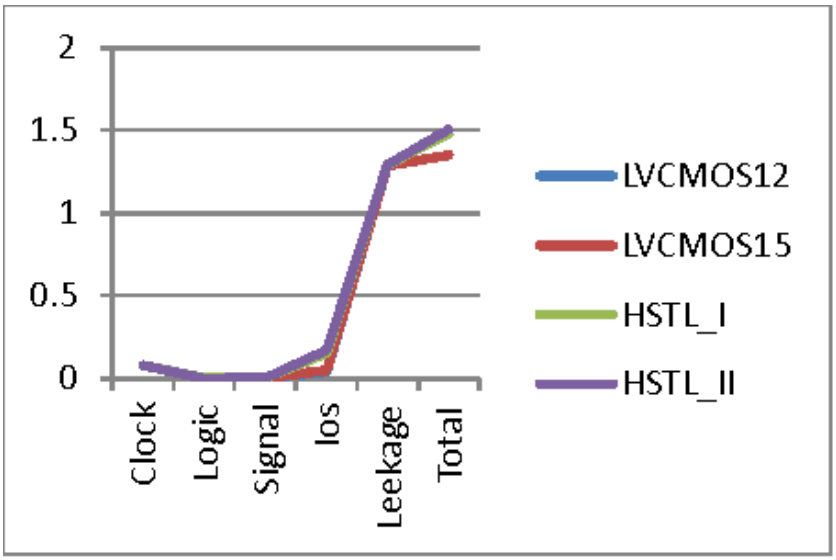

Figure 9: Power Dissipation by LED Display on 1.2 GHz

At 1.2GHz there is a reduction of 85.20% reduction in the Ios Power, 0.172% reduction in the leekage power and thus 10.20% reduction in the total power when we use LVCMOS12 instead of HSTL_I.

POWER DISSIPATION BY LED DISPLAY AT 1.7 GHZ OPERATING FREQUENCY

In this we are working on 1.7 GHz operating Frequency and we are calculating power using different variant of two IO standards (LVCMOS and HSTL).

Table 6: Power Dissipation by an LED display at 1.7 GHz

IO Standard	Clock	Logic	Signal	Ios	Leekage	Total
LVCMOS12	0.051	0.001	0.003	0.043	1.286	1.351
LVCMOS15	0.051	0.001	0.003	0.043	1.286	1.349
HSTL_I	0.051	0.001	0.003	0.15	1.291	1.477
HSTL_II	0.051	0..001	0.003	0.17	1.291	1.505

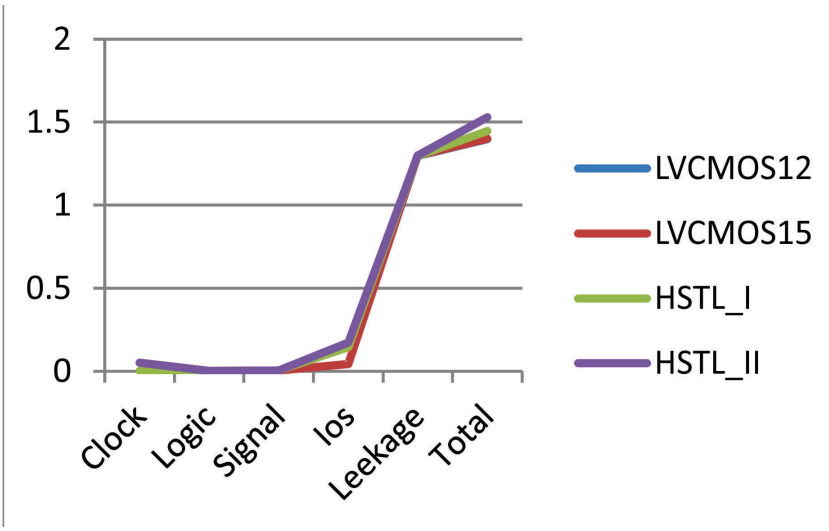

Figure10: Power Dissipation LED Display1.7 GHZ

At 1.7 GHz there is a reduction of 95.90% in the clock power, 73.27% reduction in the Ios power, 0.308% reduction in the leakage power and thus 9.13% reduction in the total power when we use LVCMOS12 instead of HSTL_I.

POWER DISSIPATED BY DISPLAY AT 2.5 GHZ OPERATING FREQUENCY

There are different IO standards available in FPGA. Power dissipation of design depends on the choice of IO standard. This is the reason behind selecting the most energy efficient IO standard in complete family of FPGA. The below shown table shows the Power dissipation at 2.5 GHz operating Frequency.

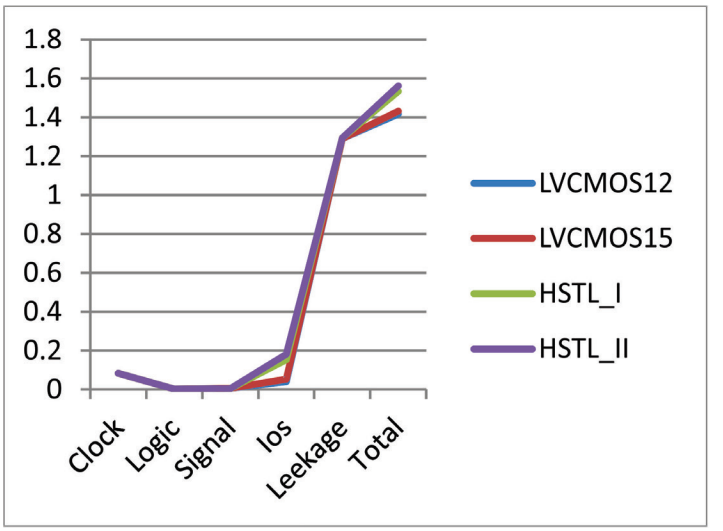

Figure11: Power Dissipation LED Display2.5GHz

At 2.5GHz there is a reduction of 30.33% in the signal power, 73.04% reduction in the Ios power, 0.302% reduction in the leakage power and thus 9.15% reduction in the total power when we use LVCMOS12 instead of HSTL_I.

CONCLUSION AND FUTURE SCOPE

Conclusion

In the time if high Performance Energy Efficient Computing (HPEEC), the center of exploration is again moving towards Eco-Friendly outline. Eco-Friendly outline helps making eco-friendly devices thus accomplishing the objective of energy efficiency. In this work we have two diverse PC components as shown in **table7.**

PC Component	Power dissipated at 3.6 GHz using LVCMOS12
Processor	1.130
LED Display	1.470

A technique named process variation has been used on the above defines PC components for these IO standards (LVCMOS and HSTL) on different operation frequencies () to find out the least power consumption and the best IO standard among them is selected. All this work is carried out at 40 nm

FPGA. According to analysis LVCMOS is the best IO standard for maximum devices. It is observer that the operating frequency is directly proportional to the power dissipated. So due to allthis our devices becomes eco-friendly.

FUTURE SCOPE

High Performance and speed is an intrinsic feature of the PC components thus designed. We have designed a few energy efficient PC components. Other PC components can also be designed like processor, RAM, antenna, graphic card etc. These devices has been implemented on 40 nm FPGA. Instead of 40 NM FRGA the design could have been implemented on 27 nm, 64 nm and 91 nm.

We use LVCMOS and HSTL I/O standards we can possibly remodify the code using other IO standards such as GTL, PCIX, PCI33 and many other I/O standards for making an energy efficient devices. Other operating frequencies can also be possibly used to test the PC Components.

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